Design and Experimental Demonstration of Novel Optical Router Controller Capable of Asynchronous, Variable-Length Packet Switching and Contention Resolution

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Abstract: This paper proposes the efficient design and implementation of a hierarchical optical router controller supporting asynchronous, variable-length optical packets. A network testbed experiment demonstrates very effective switching and contention resolution of asynchronous, variable-length optical packets.

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1. Introduction

Switching asynchronous, variable-length packets directly in the optical router data plane greatly simplifies the router data plane architecture and reduces processing overhead rising from synchronization, optical-electrical-optical (O/E/O) conversion, and repeated segmentation and reassembly of variable-length optical packets at each hop [1,2]. On the other hand, new challenges arise in designing the control plane to support asynchronous, variable-length packet switching. In particular, significant challenges lie in resolving contention, which occurs when more than one packet attempts to access the same output port on the same wavelength at the same time [1]. This paper proposes the design, implementation, and simulation of a novel optical router controller incorporating fast, fair, and wavelength-aware arbiters and an efficient contention resolution algorithm for asynchronous, variable-length optical packet switching. With an optical label switching (OLS) network testbed connected by in-ground field fibers, we demonstrate the controller for a field OLS network testbed trial in support of all-optical switching and contention resolution of asynchronously arriving, variable-length packets.

2.Design of Optical Router Controller for Asynchronous, Variable-Length Packet Switching

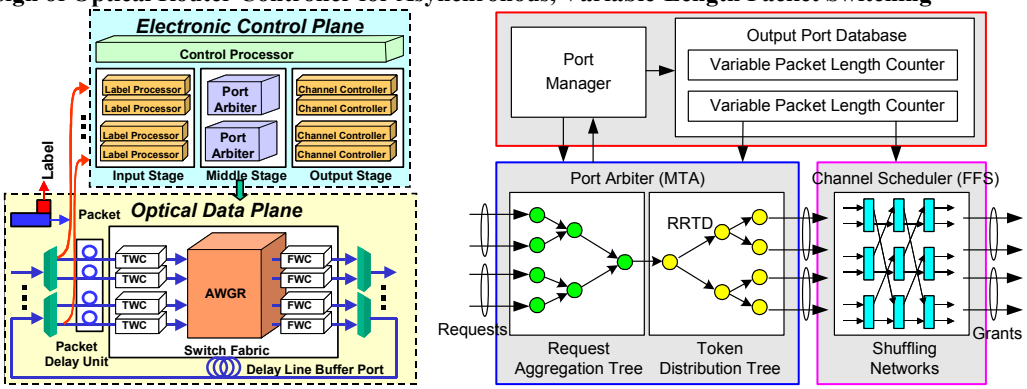


Fig. 1. A schematic of (a) an optical router architecture, (b) a middle stage port arbiter and port manager structure.

2.1 Optical Router Controller Architecture

Fig. 1 shows the optical router data plane, which consists of tunable wavelength converters (TWCs), arrayed-waveguide-grating-router (AWGR), fixed wavelength converters (FWCs), and fiber delay line buffer based optical switch fabric [2]. When an optical packet arrives, its label is extracted and sent to the electronic control plane for processing, while its packet payload travels through the data plane packet delay unit (fiber delay line) to compensate for the label processing time (~600 nsec). The proposed optical router controller sits in the electronic control plane and makes switching decisions based on the label content to reconfigure the data plane optical switch fabric in order to forward the packet to the desired output port. The proposed three-stage optical router controller consists of the input stage label processor array to process input labels, the middle stage port arbiter and manager array to make switch decisions, the output stage channel controller array to output switch fabric reconfiguration signals and generate new labels, and one additional control processor to compute the routing path and interface with the network management plane.

2.2 Input Stage Label Processor Array: Enabling Asynchronous Label Processing

Each label processor consists of a serial-to-parallel bit converter, a preamble detector, a label field analyzer, a forwarding table search engine, a contention resolution engine, and a forwarding request generator. To accommodate the data plane asynchronously arriving traffic, the preamble detector of the label processor enables immediate recognition and process of input labels. Once the preamble detector detects a valid label, the label processor will start to analyze the label content, determine the incoming packet's first and second preferred output ports, and sends forwarding request to the corresponding output port arbiter in the middle stage.

2.3 Middle Stage Port Arbiter and Manager Array: Fast, Fair, and Wavelength-Aware Switch Fabric Arbitration with Variable-length Packets Support

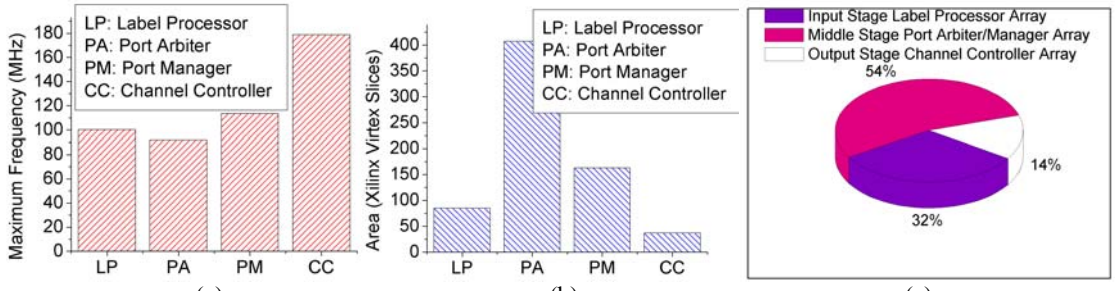
The port arbiter receives forwarding requests from input stage label processors and determines which requests to grant based on the output channel availability status provided by the port manager. The granted labels will be sent to the output stage for further processing. For asynchronously arriving packets, arbiters are necessary to schedule optical packets arriving within the same arbitration cycle in a batch to facilitate efficient hardware implementation. Fig. 1 (b) shows the port arbiter contains a mixed tree arbiter (MTA) and a shuffling-network based first-fit scheduler (FFS). The proposed arbiter achieves *fast arbitration* by utilizing both the request aggregation binary tree to aggregate forwarding requests and the reversed token distribution binary tree to distribute the available output wavelength channels, *i.e.*, the tokens, among input requests. The arbiter achieves *fair arbitration* by fairly distributing available tokens among input forwarding requests with the help of a cluster of distributed round robin token distributors (RRTD). The output channel scheduler FFS simultaneously schedules multiple incoming packets to output channels over the same output port, achieving *wavelength-aware arbitration* by fully taking advantage of the wavelength domain WDM channels to resolve packet contention. The port manager maintains a specific packet length database to support *variable-length packet switching*.

2.4 Output Stage Channel Controller Array: Facilitating Asynchronous Switch Fabric Reconfiguration

The output channel controller contains a wavelength lookup table to store switch fabric reconfiguration information, a programmable counter to determine when to reconfigure the switch fabric, and a new label generator for label swapping. To adapt the asynchronous packet traffic, the output channel controller utilizes the programmable counter to reconfigure the data plane optical switch fabric and establishes a connection inside the switch fabric before the payload packets exiting from the packet delay unit enter the switch fabric.

2.5 Optical Router Controller Hardware-Efficient Prototyping and Implementation

We prototyped the proposed controller on one Xilinx XCV1000E field programmable gate array (FPGA) chip, assuming 4 pair fiber ports and each carrying 4 wavelengths. The controller consists of 16 label processors, 4 port arbiters, 4 port managers, and 16 channel controllers. Fig. 2 (a) shows the maximum frequency of each individual module. Fig. 2 (b) shows the FPGA resources each individual module consumes in terms of Xilinx Virtex slices. Fig. 2 (c) shows the contributions of stage to the total area the optical router controller takes, where the middle stage port arbiter and manager array take the largest portion, about 38% of the total controller area. The optical router controller uses 3886 slices, about 25% of the total resource available on Xilinx XCV1000E.

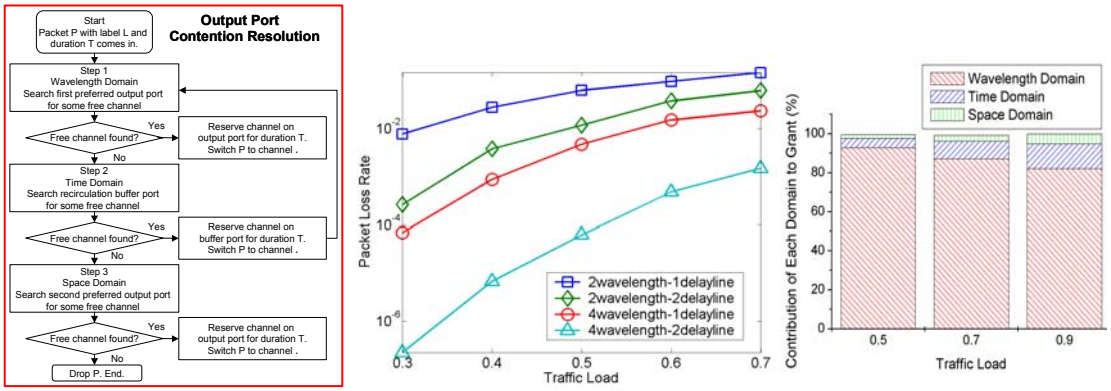


(a) (b) (c)

Fig. 2. (a) Maximum frequency, (b) FPGA area, (c) contribution of each stage to the total controller FPGA area.

3. Optical Router Controller Contention Resolution Algorithm and Simulation

The optical router controller applies contention resolution methods in wavelength [3], time [4], and space [5] domains sequentially to resolve the output port contention, when multiple incoming optical packets contend for the same switch fabric output port. Fig. 3 (a) shows the flow chart, where the controller attempts to forward the contending packets by an alternate wavelength, by delay line buffer, or by an alternate path. Fig. 3 (b) shows that the packet loss rate drops greatly as the number of wavelengths per port increases from 2 to 4 and the number of fiber delay lines increases from 1 to 2. Fig. 3 (c) demonstrates that the contribution of each contention resolution method in resolving output port contention, *i.e.*, granting the input forwarding requests, where the wavelength domain contention resolution method resolves the vast majority of the packet contention cases. As the traffic load increases from 0.5 to 0.9, the algorithm relies more on the time and the space domain methods.

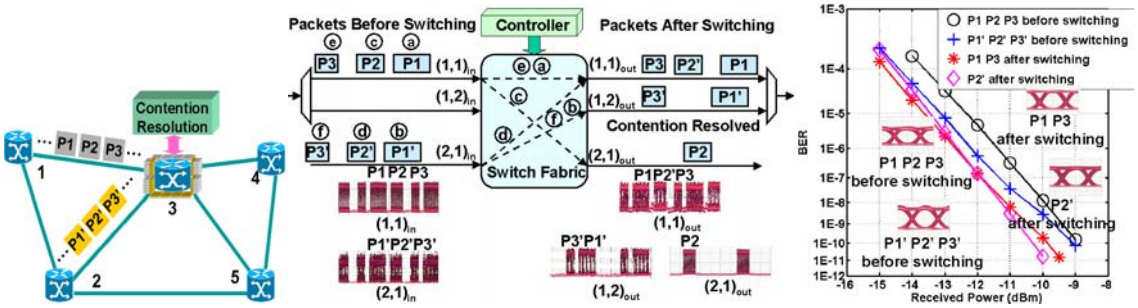


(a) (b) (c)

Fig. 3. (a) Contention resolution algorithm, (b) packet loss rate, (c) contribution of each domain to overall grant ratios.

4. Experiment of Asynchronous, Variable-Length Packet Contention Resolution with In-Ground Fibers

We emulate an OLS network testbed by connecting OLS nodes using in-ground field fibers. With this testbed, we demonstrate error-free field network testbed trial of all-optical contention resolution of asynchronously arriving, variable-length packets. Fig. 4 (a) illustrates the network topology emulated in the experimental demonstration. The OLS Node 1 and Node 2 generate asynchronous, variable-length optical packets. The packet length field in the label is a 4-bit value supporting 16 different lengths. This experiment employs 3 of them: 9216 bits, 8192 bits, and 5120 bits. The longest guard-time between packets is 206 ns. The asynchronous, variable-length packets generated in both Node 1 and 2 are destined for Nodes 4 and 5 so that contention rises at Node 3. The optical router controller at Node 3 resolves contention in the wavelength domain [1] by wavelength conversion. Fig. 4 (b) illustrates the packet sequences before and after switching at Node 3. Here, $(m, n)_{IN}$ stands for n-th wavelength channel on the m-th input fiber, while a similar definition applies for output $(m, n)_{OUT}$. The 1st output fiber is connected to Node 4, and the 2nd output fiber is to Node 5. Packet P1 from $(1, 1)_{IN}$ occupies $(1, 1)_{OUT}$ while P1' from $(2, 1)_{IN}$ arrives, P1' cannot access $(1, 1)_{OUT}$. Instead it reaches $(1, 2)_{OUT}$ on the same output fiber. When P1 has been forwarded, $(1, 1)_{OUT}$ is released since P2 targets $(2, 1)_{OUT}$. Hence, P2' is forwarded to $(1, 1)_{OUT}$. When P3 arrives, it occupies $(1, 1)_{OUT}$ again, and P3' is forwarded to $(1, 2)_{OUT}$. The controller converts the contending packets to another wavelength on the same output fiber [4]. Fig. 4 (b) shows that the controller successfully resolves contention. Fig. 4 (c) further shows BER results are error-free.



(a) (b) (c)

Fig. 4. (a) Experimental network topology, (b) packet sequences at Node 3, (c) BER results and eye-diagrams.

5. Conclusion

This paper proposes a novel optical router controller incorporating fast, fair, and wavelength-aware optical switch fabric arbitration. The design, implementation, simulation, and network testbed experiment with in-ground field fibers verify the effectiveness of the proposed controller in switching of asynchronous, variable length packets while achieving successful contention resolution.

6. References

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